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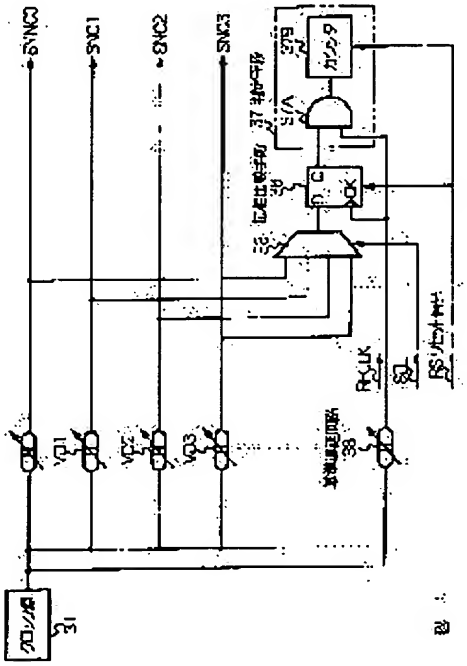
(54) METHOD AND DEVICE FOR CALIBRATING TIMING PHASE FOR DEVICE FOR TESTING SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To calibrate a lag time of each variable delay circuit for generating timing in a condition near to an actual operation to maintain a calibrated value in the practical operation.
SOLUTION: A reference clock RFCLK having the calibrated lag time is generated in a timing generator of a semiconductor device testing device, the reference clock RFCLK is phase-compared with calibrated clocks SNC1, SNC2, SNC3, etc., by a phase comparing means 36, and lag times of the variable delay circuits VD1, VD2, VD3, etc., provided in supply lines for the calibrated clocks SNC1, SNC2, SNC3, etc., are set to be conformed with phase comparison results therein.



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